**Interrupt Controller with APB Interface**

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**Specification**

Introduction

Interrupt Controller with APB Interface is a module that is used to combine several sources of interrupt into one single line, allowing priority levels to the interrupt input lines. The controller registers are configured via the AMBA 3 APB Protocol.

Features

* detects, stores and deals with interrupt pulses
* the module has four interrupt lines
* 4 bit Status Register for incoming interrupt status bits and pending interrupt status
* 4 bit configurable Mask Register for interrupt enables, this register specifies which interrupt are to be ignored and not acknowledged
* 4 bit configurable Clear Register, this register is configured to delete the interrupts that have been served from the status register
* full AMBA 3 APB Interface
* asynchronous reset, active LOW
* enable signal for clock gating, to reduce dynamic power dissipation by removing the clock signal when the circuit is not in use

Interrupt Controller Interface

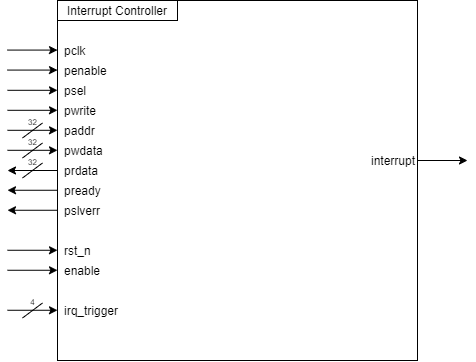


Figure Interrupt Controller Symbol

Signals Table

Table Signals Table

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Signal | Direction | Nr. of lines | Description | Active |
| pclk | input | 1 | clock | rising edge |
| penable | input | 1 | indicates the second cycle of an APB transfer | HIGH |
| psel | input | 1 | select to bus slave | HIGH |
| pwrite | input | 1 | write or read acces | HIGH w/LOW r |
| paddr | input | 32 | APB address bus | - |
| pwdata | input | 32 | APB write data bus | - |
| prdata | output | 32 | APB read data bus | - |
| pready | output | 1 | extend APB transfer | LOW |
| pslverr | output | 1 | indicates a transfer failure | HIGH |
| rst\_n | input | 1 | asynchronous reset | LOW |
| enable | input | 1 | clock gating enable | HIGH |
| irq\_trigger | input | 4 | interrupt requests | pulse HIGH |
| interrupt | output | 1 | interrupt | HIGH |

Implementation

Interrupt Controller has the following set of registers: Status Register, Mask Register, Clear Register. The Status Register specifies which interrupt request lines received trigger pulses, this happens through a block that detects the rising edges of the pulses. The Mask Register is a configurable register that specifies the priority of the interrupt request lines. By configuring the Clear Register, the clear function is performed through all the registers.

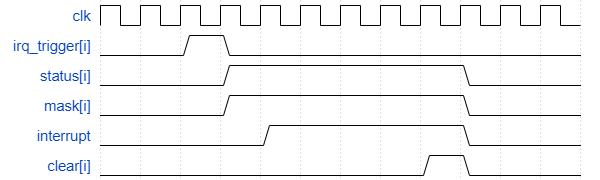


Figure Interrupt Controller registers behavior

The configuration of the registers takes place through the APB interface, which is used to set the priority of the interrupt request lines, and to clear the registers when the interrupt has been served. Figure 3 shows the block diagram of the Interrupt Controller.

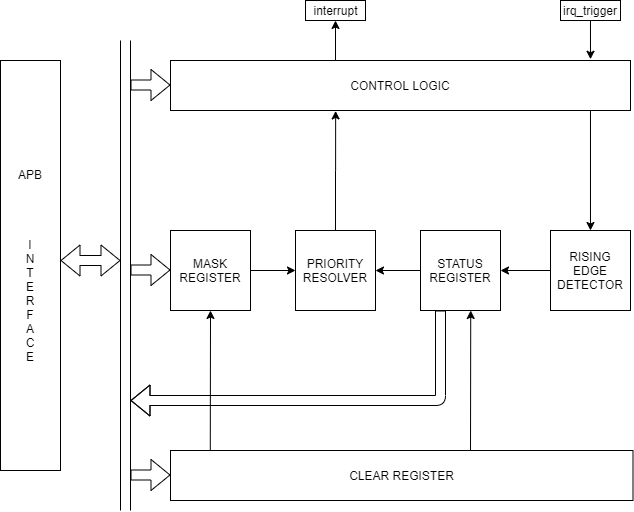


Figure Interrupt Controller block diagram